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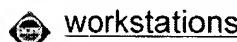**181 High-level synthesis of scalable architectures for IIR filters using multichip modules**   ▬
Haigeng Wang, Nikil Dutt, Alexandru Nicolau, Kai-Yeung Sunny Siu
July 1993 **Proceedings of the 30th international conference on Design automation**
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182 Session 14: cluster computing: NAS experiences with a prototype cluster of workstations   ▬
K. Castagnera, D. Cheng, R. Fatoohi, E. Hook, B. Kramer, C. Manning, J. Musch, C. Niggley, W. Saphir, D. Sheppard, M. Smith, I. Stockdale, S. Welch, R. Williams, D. Yip
November 1994 **Proceedings of the 1994 ACM/IEEE conference on Supercomputing**
Publisher: ACM Press
Full text available: ▣ pdf(987.83 KB)   Additional Information: full citation, abstract, references

This paper discusses the year-long activity at NAS to implement a large, loose cluster of workstations from the existing Silicon Graphics, Inc. (SGI) pool of systems. Issues related to establishing a loosely coupled cluster of workstations are presented. Included are steps needed to resolve system management issues intended to provided reasonable cycle recovery from these systems without disrupting the primary system users. Performance evaluation tests were run based on the NAS Parallel Benchmar ...

183 ByteLisp and its Alto implementation   ▬
L. Peter Deutsch
August 1980 **Proceedings of the 1980 ACM conference on LISP and functional programming**
Publisher: ACM Press
Full text available: ▣ pdf(989.19 KB)   Additional Information: full citation, abstract, references, citings, index terms

This paper describes in detail the most interesting aspects of ByteLisp, a transportable Lisp system architecture which implements the Interlisp dialect of Lisp, and its first implementation, on a microprogrammed minicomputer called the Alto. Two forthcoming related papers will deal with general questions of Lisp machine and system architecture, and detailed measurements of the Alto ByteLisp system described here. A highly condensed summary of the series was published at MICRO-11 in Novembe ...

184 Compiler and hardware support for cache coherence in large-scale multiprocessors: design considerations and performance study   ▬
Lynn Choi, Pen-Chung Yew
May 1996 **ACM SIGARCH Computer Architecture News , Proceedings of the 23rd**